PATENT ABSTRACTS OF JAPAN

(11) Publication number : 04-246728
(43) Date of publication of application : 02.09.1992

(51) Int.Cl. G06F 9/38
G06F 9/318
G06F 9/38

(21) Application number : 03-012191
(22) Date of filing : 01.02.1991

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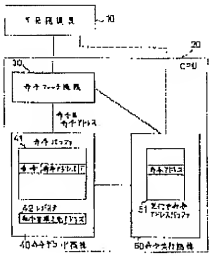
(54) INFORMATION PROCESSOR

(57) Abstract:
PURPOSE: To constitute the processor so that a software for rewriting an instruction itself is processed as expected without limiting the number of instructions inputted to an instruction buffer from a main storage.
CONSTITUTION: The processor is provided with an instruction buffer 41 in which an instruction fetched from a main storage device 10 is held by forming a pair with its instruction address, and an executive instruction address buffer 51 in which an instruction address of an executive instruction is held. An instruction executing mechanism 50 discriminates whether an instruction of an instruction rewriting destination address exists in the buffer 41 or the buffer 51 or not, and executes rewriting of the instruction concerned in the buffer 41, or refetch of the instruction after the instruction rewriting instruction in accordance with a result of its discrimination. Also, at the time of decoding the refetched instruction, when an address of its instruction coincides with an instruction rewriting destination address, an instruction decoding mechanism 40 waits for rewriting of its instruction.



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